AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions or listings of claims for this application:

Listing of Claims:

Claims 1-86 (Canceled).

87. (Previously presented) A CMOS imager having improved transistor speed comprising:

a substrate doped to a first conductivity type;

an array of pixel cells formed on said substrate, each of said cells including a photocollection region doped to a second conductivity type, at least one transistor, and a partially removed opaque conductive layer, wherein said transistor includes, over a gate region of the transistor, a remaining portion of said opaque conductive layer, and said photocollection region includes a photogate from which said opaque conductive layer has been removed; and

signal processing circuitry on said substrate, wherein said circuitry is connected to said array.

88. (Previously presented) The CMOS imager according to claim 87, wherein said opaque conductive layer is an opaque conductive silicide layer.

89. (Previously presented) The CMOS imager according to claim 87, wherein said opaque conductive layer is an opaque conductive barrier metal layer.

90. (Previously presented) The CMOS imager according to claim 88, wherein said opaque conductive silicide layer is a tungsten silicide.

91. (Previously presented) The CMOS imager according to claim 88, wherein said opaque conductive silicide layer is a titanium silicide.

92. (Previously presented) The CMOS imager according to claim 88, wherein said opaque conductive silicide layer is a cobalt silicide.

93. (Previously presented) The CMOS imager according to claim 88, wherein said opaque conductive silicide layer is a molybdenum silicide.

94. (Previously presented) The CMOS imager according to claim 89, wherein said opaque conductive barrier metal layer is a TiN/W layer.

95. (Previously presented) The CMOS imager according to claim 89, wherein said opaque conductive barrier metal layer is a WN_x/W layer.

96. (Previously presented) The CMOS imager according to claim 89, wherein said opaque conductive barrier metal layer is a WN_x layer.

97. (Previously presented) The CMOS imager according to claim 87, wherein said transistor is one or more of a reset transistor, a row

select transistor, source follower transistor, amplifier transistor or a transfer transistor.

98. (Previously presented) The CMOS imager according to claim 87, wherein said transistor is a reset transistor.

99. (Previously presented) The CMOS imager according to claim 98, further comprising a transfer transistor to transfer charge from said photocollection region to said signal processing circuitry, wherein said transfer transistor includes an opaque conductive layer deposited over the gate region of said transistor.

100. (Previously presented) The CMOS imager according to claim 87, wherein said imager further includes a thin ring of opaque conductive layer formed over the outer periphery of said photogate.

101. (Previously presented) The CMOS imager according to claim 100, wherein said imager further includes a light shield formed over said imager such that said light shield does not cover a substantial portion of said photocollection region.

102. (Previously presented) A processing system comprising:

(i) a processor; and

(ii) a CMOS imaging device coupled to said processor and including:

a substrate doped to a first conductivity type;

an array of pixel cells formed on said substrate, each of said cells including a photocollection region doped to a second conductivity type, at least one transistor, and a partially removed opaque conductive layer, wherein said transistor includes, over a gate region of the transistor, a remaining portion of said opaque conductive layer, and said photocollection region includes a photogate from which said opaque conductive layer has been removed; and

signal processing circuitry on said substrate, wherein said circuitry is connected to said array.

103. (Previously presented) The system according to claim 102, wherein said opaque conductive layer is an opaque conductive silicide layer.

104. (Previously presented) The system according to claim 102, wherein said opaque conductive layer is an opaque conductive barrier metal layer.

105. (Previously presented) The system according to claim 103, wherein said opaque conductive silicide layer is a tungsten silicide.

106. (Previously presented) The system according to claim 103, wherein said opaque conductive silicide layer is a titanium silicide.

107. (Previously presented) The system according to claim 103, wherein said opaque conductive silicide layer is a cobalt silicide.

108. (Previously presented) The system according to claim 103, wherein said opaque conductive silicide layer is a molybdenum silicide.

109. (Previously presented) The system according to claim 104, wherein said opaque conductive barrier metal layer is a TiN/W layer.

110. (Previously presented) The system according to claim 104, wherein said opaque conductive barrier metal layer is a WN_x/W layer.

111. (Previously presented) The system according to claim 104, wherein said opaque conductive barrier metal layer is a WN_x layer.

112. (Previously presented) The system according to claim 102, wherein said transistor is one or more of a reset transistor, a row select transistor, an amplifying transistor, a source follower transistor or a transfer transistor.

113. (Previously presented) The system according to claim 102, wherein said transistor is a reset transistor.

114. (Previously presented) The system according to claim 113, further comprising a transfer transistor to transfer charge from said photocollection region to said signal processing circuitry, wherein said transfer transistor includes an opaque conductive layer deposited over the gate region of said transistor.

115. (Previously presented) The system according to claim 102, wherein said imager further includes a thin ring of opaque conductive layer formed over the outer periphery of said photogate.

116. (Previously presented) The system according to claim 115, wherein said imager further includes a light shield formed over said

imager such that said light shield does not cover a substantial portion of said photocollection region.

117. (Previously presented) A CMOS imager having improved transistor speed comprising:

a substrate doped to a first conductivity type;

an array of pixel cells formed on said substrate, each of said cells including a photocollection region doped to a second conductivity type with an etched photogate, and at least one transistor having a portion of a deposited opaque conductive layer over a gate region of the transistor; and

signal processing circuitry on said substrate, wherein said circuitry is connected to said array,

wherein said photogate is void of said deposited opaque conductive layer.

118. (Previously presented) A processing system comprising:

(i) a processor; and

(ii) a CMOS imaging device coupled to said processor and including:

a substrate doped to a first conductivity type;

an array of pixel cells formed on said substrate, each of said cells including a photocollection region doped to a second conductivity type with an etched

photogate, and at least one transistor having a portion of a deposited opaque conductive layer over a gate region of the transistor; and

signal processing circuitry on said substrate, wherein said circuitry is connected to said array,

wherein said photogate is void of said deposited opaque conductive layer.

119. (Previously presented) A CMOS imager having improved transistor speed comprising:

a substrate; and

an array of pixel cells formed on said substrate, each of said cells including a photogate, a transfer gate, a reset gate, and a partially removed opaque conductive layer, wherein a remaining portion of said opaque conductive layer remains over said transfer gate and said reset gate, and wherein said photogate is void of said opaque conductive layer.

120. (Previously presented) The CMOS imager according to claim 119, wherein said opaque conductive layer is an opaque conductive silicide layer.

121. (Previously presented) The CMOS imager according to claim 119, wherein said opaque conductive layer is an opaque conductive barrier metal layer.

122. (Previously presented) The CMOS imager according to claim 120, wherein said opaque conductive silicide layer is a tungsten silicide.

123. (Previously presented) The CMOS imager according to claim 120, wherein said opaque conductive silicide layer is a titanium silicide.

124. (Previously presented) The CMOS imager according to claim 120, wherein said opaque conductive silicide layer is a cobalt silicide.

125. (Previously presented) The CMOS imager according to claim 120, wherein said opaque conductive silicide layer is a molybdenum silicide.

126. (Previously presented) The CMOS imager according to claim 121, wherein said opaque conductive barrier metal layer is a TiN/W layer.

127. (Previously presented) The CMOS imager according to claim 121, wherein said opaque conductive barrier metal layer is a WN_x/W layer.

128. (Previously presented) The CMOS imager according to claim 121, wherein said opaque conductive barrier metal layer is a WN_x layer.